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FORM PTO-1449 (Modified LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT Page 1 of 4 (Use several sheets if necessary)	ATTY. DOCKET NO. RPS920010127US1	SERIAL NO. 10/016,449
	APPLICANT: R. T. Bailis, et al.	
	FILING DATE: 12/10/2001	GROUP: 2133

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
JJJ	6 1 3 4 1 7 3	Oct. 17, 2000	Cliff, et al.	265	230.03	Nov. 2, 1998
JJJ	6 1 7 3 4 1 9B1	Jan. 9, 2001	Barnett	714	28	May 14, 1998
JJJ	6 1 7 8 5 4 1B1	Jan. 23, 2001	Joly, et al.	716	17	Mar. 30, 1998
JJJ	6 1 8 1 1 5 9B1	Jan. 20, 2001	Rangasayee	326	39	Aug. 25, 1998
JJJ	6 1 8 2 2 0 6B1	Jan. 30, 2001	Baxter	712	43	Feb. 26, 1998
JJJ	6 1 8 2 2 4 7B1	Jan. 30, 2001	Hermann, et al.	714	39	Oct. 27, 1997

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

JJJ BB	C. E. Kuhlmann et al., U.S. Pending Patent Application Serial No. 10/016346 (docket RPS920010125US1), "Field Programmable Network Processor and Method for Customizing a Network Processor"
JJJ CC	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/016772 (docket RPS920010126US1), "Method and System for Use of an Embedded Field Programmable Gate Array Interconnect for Flexible I/O Connectivity"

EXAMINER	DATE CONSIDERED
John J. Tabone, Jr.	4/5/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
JJZ	6 1 9 1 6 1 4B1	Feb. 20, 2001	Schultz, et al.	326	41	Aug. 13, 1999
JJZ	6 2 0 9 1 1 8B1	Mar. 27, 2001	LaBerge	716	1	Jan. 21, 1998
JJZ	6 2 1 1 6 9 7B1	Apr. 3, 2001	Lien, et al.	326	41	May 25, 1999
JJZ	6 2 1 9 8 1 9B1	Apr. 17, 2001	Vashi, et al.	716	3	Jun. 26, 1998
JJZ	6 2 1 9 8 3 3B1	Apr. 17, 2001	Solomon, et al.	717	5	Dec. 11, 1998
JJZ	6 2 2 3 1 4 8	Apr. 24, 2001	Stewart, et al.	703	25	Aug. 14, 1998

FOREIGN PATENT DOCUMENTS

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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

JJZ DD	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/016448 (docket RPS920010128US1), "Method and System for Use of a Field Programmable Function within an Application Specific Integrated Circuit (ASIC) to Access Internal Signals for External Observation and Control"
JJZ EE	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015922 (docket RPS920010129US1), "Method and System for Use of a Field Programmable Interconnect within an ASIC for Configuring the ASIC"

EXAMINER	DATE CONSIDERED
John J. Tabone, Jr.	4/5/04

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
JJJ	6 2 2 3 3 1 3B1	Apr. 24, 2001	How, et al.	714	724	Dec. 5, 1997
JJJ	6 2 2 6 7 7 6B1	May 1, 2001	Panchul, et al.	716	3	Sep. 16, 1997
JJJ	6 2 3 0 1 1 9B1	May 8, 2001	Mitchell	703	27	Feb. 6, 1998
JJJ	6 2 3 7 0 2 1B1	May 22, 2001	Drummond	709	201	Sep 25, 1998
JJJ	6 2 4 7 1 4 7B1	Jun. 12, 2001	Beenstra, et al.	714	39	Jun. 12, 2001
JJJ	6 2 4 9 1 4 3B1	Jun. 19, 2001	Zaveri, et al.	326	40	Jan. 15, 1998

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JJJ FF	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015920 (docket RPS920010130US1), "Method and System for Use of a Field Programmable Function within a Chip to Enable Configurable I/O Signal Timing Characteristics"
JJJ GG	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015923 (docket RPS920010131US1), "Method and System for Use of a Field Programmable Function within a Standard Cell Chip for Repair of Logic Circuits"

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
JJ	6 2 5 2 4 2 2B1	Jun. 26, 2001	Patel, et al.	326	80	Sep. 22, 1999
JJ	6 2 5 3 2 6 7B1	Jun. 26, 2001	Kim, et al.	710	103	Jul. 31, 1998
JJ	6 2 5 6 2 9 6B1	Jul. 3, 2001	Ruziak, et al.	370	277	Dec. 17, 1997
JJ	6 2 6 0 0 8 7B1	Jul. 10, 2001	Chang	710	100	Mar. 3, 1999
JJ	6 2 6 0 1 8 2B1	Jul. 10, 2001	Mohan, et al.	716	12	Mar. 27, 1998
JJ	6 2 6 0 1 8 5B1	Jul. 10, 2001	Sasaki, et al.	716	18	Apr. 24, 1996

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						YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

JJ HH	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015921 (docket RPS920010132US1), "Method and System for Use of a Field Programmable Gate Array (FPGA) Cell for Controlling Access to On-Chip Functions of a System on a Chip (SOC) Integrated Circuit"

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